each level of partitioning. Other approaches to the partitioning process include min-cut, force-directed, simulated annealing, and spectral approaches. --

IN THE CLAIMS

Please cancel claims 1-14 and 18-21 without prejudice, and replace with claims 22-36 as shown below.

1 22. In the design of integrated circuits, a computer controlled method for placing cells in a placement area, comprising:

generating a netlist through a synthesis process;

establishing a convergence criterion based upon a partition size;

executing a cell separation process according to the netlist:

changing the netlist in response to how the cells are placed;

modifying the spacings of the cells responsive to changes made to the netlist;

partitioning the cells into a plurality of partitions; and,

determining whether the partitions meet said criterion for convergence.

2 23. The method of claim 22, further comprising inputting HDL, user constraints, and technology data into the synthesis process for generating the netlist.

3 24. The method of claim 22 wherein a change to the netlist includes sizing a gate up or down.

4 25. The method of claim 22 wherein a change to the netlist includes adding or deleting one or more gates.

5 1

26. The method of claim 22 wherein the partition size is measured by the number of gates contained therein.

4

27. In the design of integrated circuits, a computer controlled method for placing cells in a placement area, comprising:

generating a netlist through a synthesis process;

establishing a convergence criterion based upon a partition size;

executing a cell separation process according to the netlist;

changing the netlist;

changing the size of said placement area;

modifying the spacings of the cells responsive to changes made to the netlist;

partitioning the cells into a plurality of partitions; and,

determining whether the partitions meet said criterion for convergence.

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28. The method of claim 27, further comprising inputting HDL, user constraints, and technology data into the synthesis process for generating the netlist.

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29. The method of claim 27 wherein a change to the netlist includes sizing a gate up or down.

9 4

30. The method of claim 27 wherein a change to the netlist includes adding or deleting one or more gates.

10 4

31. The method of claim 27 wherein the partition size is measured by the number of gates contained.

D

11
~~32.~~ In the design of integrated circuits, a computer controlled method for placing cells in a placement area, comprising:

generating a netlist through a synthesis process;

establishing a convergence criterion based upon a partition size;

executing a cell separation process according to the netlist:

changing the netlist in response how the cells are placed;

changing the size of said placement area;

modifying the spacings of the cells responsive to changes made to the netlist;

partitioning the cells into a plurality of partitions; and,

determining whether the partitions meet said criterion for convergence.

12 11
~~33.~~ The method of claim ~~22~~ 32, further comprising inputting HDL, user constraints, and technology data into the synthesis process for generating the netlist.

13 11
~~34.~~ The method of claim ~~22~~ 32 wherein a change to the netlist includes sizing a gate up or down.

14 11
~~35.~~ The method of claim ~~22~~ 32 wherein a change to the netlist includes adding or deleting one or more gates.

15 11
~~36.~~ The method of claim ~~22~~ 32 wherein the partition size is measured by the number of gates contained.